PATENT ABSTRACTS OF JAPAN

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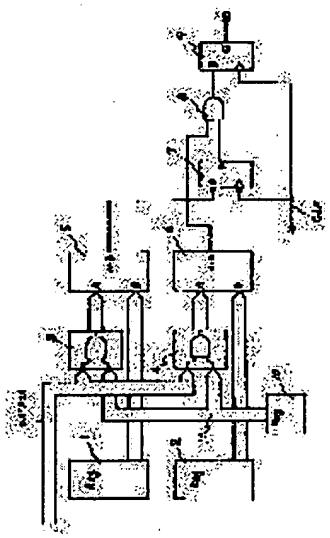
(54) TRIGGER SIGNAL GENERATION CIRCUIT

(57)Abstract:

PURPOSE: To enable the generation of a trigger signal both as such to be created sequentially and as unable to be determined primarily, by having the results of comparison of a first comparator circuit ANDed with the results of comparison of a second comprator circuit by an AND circuit once delayed by a fixed time to obtain a trigger signal.



CONSTITUTION: An input signal DATAIN is inputted into comparator circuits 5 and 6 as maskable in LSB side bits with AND gate groups 3 and 4 on the basis of data from a mask register 10 while trigger conditions are inputted into the circuits 5 and 6 from registers 1 and 2 and the comparator circuits 5 and 6 compare the signal DATAIN with the trigger condition. After being set on a D type FF7 in which a clock signal CLK synchronous to the signal DATAIN is already inputted as a setting signal, the results of comparison from the circuit 5 are ANDed with the results of comparison from the circuit 6 by an AND gate 8. Thus, a D type FF9 is allowed to be set only when the AND output of '1' is obtained from the AND gate 8 and the set output given at this time is obtained as a trigger signal.

LEGAL STATUS

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